

What is claimed is:

- 1           1. A serial digital signal transmission system comprising
- 2    a residual time stamp (RTS) generator circuit for separating
- 3    high definition television (HDTV) serial digital signals to be
- 4    transmitted into parallel data and time information residual
- 5    time stamps (RTSs) and transmitting them as separated, and an
- 6    RTS receiver circuit for receiving said parallel data and said
- 7    time information RTSs that have been transmitted and obtaining
- 8    said HDTV serial digital signals as they were originally,
- 9    wherein:
- 10           said RTS generator circuit has:
- 11            first frequency dividing means for dividing a network clock
- 12           into a prescribed first frequency,
- 13            a serial-to-parallel converter for subjecting said HDTV
- 14           serial digital signals to be transmitted to serial-to-parallel
- 15           conversion, transmitting data of the resultant parallel signals
- 16           and supplying a clock divided into a second frequency,
- 17            a first counter for dividing said frequency-divided clock
- 18           supplied from said serial-to-parallel converter into a  $1/N$
- 19           frequency, and
- 20            a latch circuit for latching at the output timing of said
- 21           first counter the clock resulting from the frequency division
- 22           by said first frequency dividing means to supply said time
- 23           information RTSs, and
- 24            said RTS receiver circuit comprises:
- 25            second frequency dividing means for dividing the frequency
- 26           of said network clock into said prescribed first frequency,
- 27            gate pulse generating means for generating a gate pulse

28 on the basis of said network clock,  
29 memory means for temporarily storing said RTSs which have  
30 been transmitted,  
31 a comparator for comparing the clock resulting from  
32 frequency division by said second frequency dividing means and  
33 said RTSs read out of said memory means,  
34 a gate circuit for gating the output signal of said  
35 comparator on the basis of said gate pulse from said gate pulse  
36 generating means,  
37 frequency multiplying means for regenerating the clock  
38 of said second frequency by multiplying the frequency of the  
39 output signal of said gate circuit to said N-multiplied frequency,  
40 and  
41 a parallel-to-serial converter for receiving as its inputs  
42 regenerated clock of said second frequency supplied from said  
43 frequency multiplying means and data of said parallel signals  
44 that have been transmitted, and subjecting these to  
45 parallel-to-serial conversion to obtain said HDTV serial digital  
46 signals, 8, 15 or 16 being selected as the value of said N.

1 2. The serial digital signal transmission system, as  
2 claimed in Claim 1, wherein said first frequency dividing means  
3 comprises a first frequency dividing circuit for dividing said  
4 network clock into a frequency of  $1/32$  and a first p-bit counter  
5 for counting clocks supplied from said first frequency dividing  
6 circuit and obtaining a signal of said prescribed first frequency,  
7 said second frequency dividing means comprises a second frequency  
8 dividing circuit for dividing said network clock into a frequency

9 of 1/32 and a second p-bit counter for counting clocks supplied  
10 from said second frequency dividing circuit and obtaining a  
11 signal of said prescribed first frequency, said gate pulse  
12 generating means is an  $M_q - 2^{(p-1)}$  counter (where  $M_q$  is the largest  
13 integer that does not surpass the average count  $M'$  of the clock  
14 resulting from frequency division by 32 of the network clock  
15 in N periods of the serial clock of HDTV serial digital signals)  
16 for counting the clock supplied from said second frequency  
17 dividing circuit and supplying said gate pulse, and said  
18 frequency multiplying means is a PLL circuit for multiplying  
19 the frequency of the output signal of said gate circuit to said  
20 N-multiplied frequency.

1 3. The serial digital signal transmission system, as  
2 claimed in Claim 2, wherein said memory means is a FIFO storage  
3 whose read timing is determined by the output signal of said  
4 gate circuit and said  $M_q - 2^{(p-1)}$  counter is reset by the output  
5 signal of said gate circuit.

1 4. A serial digital signal transmission apparatus  
2 comprising a serial-to-parallel converter for separating high  
3 definition television (HDTV) serial digital signals to be  
4 transmitted into a parallel data and a first clock, a residual  
5 time stamp (RTS) generator circuit for generating time  
6 information RTSs on the basis of said first clock and a network  
7 clock, an ATM cell processing unit for assembling said RTSs and  
8 parallel data into asynchronous transfer mode (ATM) cells of  
9 a prescribed structure and transmitting the assembled cells and

10 separating received ATM cells of said prescribed structure into  
11 said RTSs and parallel data, an RTS receiver circuit for  
12 regenerating said first clock as they originally were on the  
13 basis of said separated time information RTSs and network clock,  
14 and a parallel-to-serial converter for obtaining said HDTV serial  
15 digital signals from said separated parallel data and said first  
16 clock from said RTS receiver circuit, wherein:

17       said RTS generator circuit has:

18       first frequency dividing means for dividing said network  
19 clock into a second clock of a prescribed frequency,

20       a first counter for dividing said first clock into a  $1/N$   
21 frequency, and

22       a latch circuit for latching at the output timing of said  
23 first counter the second clock resulting from the frequency  
24 division by said first frequency dividing means to supply said  
25 time information RTSs,

26       said RTS receiver circuit comprises:

27       second frequency dividing means for dividing the frequency  
28 of said network clock into said prescribed frequency,

29       gate pulse generating means for generating a gate pulse  
30 on the basis of said network clock,

31       memory means for temporarily storing said RTSs which have  
32 been transmitted,

33       a comparator for comparing the clock resulting from  
34 frequency division by said second frequency dividing means and  
35 said RTSs read out of said memory means,

36       a gate circuit for gating the output signal of said  
37 comparator on the basis of said gate pulse from said gate pulse

38 generating means, and  
39 frequency multiplying means for regenerating said first  
40 clock frequency by multiplying the frequency of the output signal  
41 of said gate circuit to said N-multiplied frequency, wherein:  
42 said ATM cell processing unit, besides selecting 8 as the  
43 value of said N, multiplexes 180 bytes of said HDTV serial digital  
44 signals on four of said ATM cells to generate ATM cells on whose  
45 remainder of payload are multiplexed nine of said time  
46 information RTSs corresponding to the 180 bytes of HDTV serial  
47 digital signals.

1 5. A serial digital signal transmission apparatus  
2 comprising a serial-to-parallel converter for separating high  
3 definition television (HDTV) serial digital signals to be  
4 transmitted into a parallel data and a first clock, a residual  
5 time stamp (RTS) generator circuit for generating time  
6 information RTSs on the basis of said first clock and a network  
7 clock, an ATM cell processing unit for assembling said RTSs and  
8 parallel data into asynchronous transfer mode (ATM) cells of  
9 a prescribed structure and transmitting the assembled cells and  
10 separating received ATM cells of said prescribed structure into  
11 said RTSs and parallel data, an RTS receiver circuit for  
12 regenerating said first clock as they originally were on the  
13 basis of said separated time information RTSs and network clock,  
14 and a parallel-to-serial converter for obtaining said HDTV serial  
15 digital signals from said separated parallel data and said first  
16 clock from said RTS receiver circuit, wherein:  
17 said RTS generator circuit has:

18 first frequency dividing means for dividing said network  
19 clock into a second clock of a prescribed frequency,  
20 a first counter for dividing said first clock into a  $1/N$   
21 frequency, and  
22 a latch circuit for latching at the output timing of said  
23 first counter the second clock resulting from the frequency  
24 division by said first frequency dividing means to supply said  
25 time information RTSS,  
26 said RTS receiver circuit comprises:  
27 second frequency dividing means for dividing the frequency  
28 of said network clock into said prescribed frequency,  
29 gate pulse generating means for generating a gate pulse  
30 on the basis of said network clock,  
31 memory means for temporarily storing said RTSS which have  
32 been transmitted,  
33 a comparator for comparing the clock resulting from  
34 frequency division by said second frequency dividing means and  
35 said RTSS read out of said memory means,  
36 a gate circuit for gating the output signal of said  
37 comparator on the basis of said gate pulse from said gate pulse  
38 generating means, and  
39 frequency multiplying means for regenerating said first  
40 clock frequency by multiplying the frequency of the output signal  
41 of said gate circuit to said  $N$ -multiplied frequency, wherein:  
42 said ATM cell processing unit, besides selecting 8 as the  
43 value of said  $N$ , multiplexes 5500 bytes of said HDTV serial digital  
44 signals on 123 of said ATM cells to generate ATM cells on whose  
45 remainder of payload are multiplexed 275 of said time information

46 RTSs corresponding to the 5500 bytes of HDTV serial digital  
47 signals.

1           6. A serial digital signal transmission apparatus  
2 comprising a serial-to-parallel converter for separating high  
3 definition television (HDTV) serial digital signals to be  
4 transmitted into a parallel data and a first clock, a residual  
5 time stamp value (RTS) generator circuit for generating time  
6 information RTSs on the basis of said first clock and a network  
7 clock, an ATM cell processing unit for assembling said RTSs and  
8 parallel data into asynchronous transfer mode (ATM) cells of  
9 a prescribed structure and transmitting the assembled cells and  
10 separating received ATM cells of said prescribed structure into  
11 said RTSs and parallel data, an RTS receiver circuit for  
12 regenerating said first clock as they originally were on the  
13 basis of said separated time information RTSs and network clock,  
14 and a parallel-to-serial converter for obtaining said HDTV serial  
15 digital signals from said separated parallel data and said first  
16 clock from said RTS receiver circuit, wherein:

17           said RTS generator circuit has:

18           first frequency dividing means for dividing said network  
19 clock into a second clock of a prescribed first frequency,

20           a first counter for dividing said first clock into a  $1/N$   
21 frequency, and

22           a latch circuit for latching at the output timing of said  
23 first counter the second clock resulting from the frequency  
24 division by said first frequency dividing means to supply said  
25 time information RTSs,

26           said RTS receiver circuit comprises:  
27           second frequency dividing means for dividing the frequency  
28 of said network clock into said prescribed frequency,  
29           gate pulse generating means for generating a gate pulse  
30 on the basis of said network clock,  
31           memory means for temporarily storing said RTSs which have  
32 been transmitted,  
33           a comparator for comparing the clock resulting from  
34 frequency division by said second frequency dividing means and  
35 said RTSs read out of said memory means,  
36           a gate circuit for gating the output signal of said  
37 comparator on the basis of said gate pulse from said gate pulse  
38 generating means, and  
39           frequency multiplying means for regenerating said first  
40 clock frequency by multiplying the frequency of the output signal  
41 of said gate circuit to said N-multiplied frequency, wherein:  
42           said ATM cell processing unit, besides selecting 15 as  
43 the value of said N, multiplexes 375 bytes of said HDTV serial  
44 digital signals on eight of said ATM cells to generate ATM cells  
45 on whose remainder of payload and RTS area of Segmentation and  
46 Reassembly Protocol Data Unit (SAR-PDU) header are multiplexed  
47 10 of said time information RTSs corresponding to the 375 bytes  
48 of HDTV serial digital signals.

1           7. A serial digital signal transmission apparatus  
2 comprising a residual time stamp (RTS) generator circuit for  
3 separating high definition television (HDTV) serial digital  
4 signals to be transmitted into parallel data and time information



5 residual time stamps (RTSs) and for transmitting said parallel  
6 data and said time as separated, and an RTS receiver circuit  
7 for receiving said parallel data and said time information RTSs,  
8 wherein said RTS generator circuit has:

9       first frequency dividing means for dividing a network clock  
10 into a prescribed first frequency,

11       a serial-to-parallel converter for subjecting said HDTV  
12 serial digital signals to be transmitted to serial-to-parallel  
13 conversion, transmitting data of the resultant parallel signals  
14 and supplying a clock divided into a second frequency,

15       a first counter for dividing said frequency-divided clock  
16 supplied from said serial-to-parallel converter into a  $1/N$   
17 frequency, and

18       a latch circuit for latching at the output timing of said  
19 first counter the clock resulting from the frequency division  
20 by said first frequency dividing means to supply said time  
21 information RTSs